REMARKS

Overview

Claims 1, 2, and 4-68 are all the claims currently pending in this Application. Claims 38-68 are withdrawn. Applicants again note that the Examiner mistakenly lists claims 1-71 as pending. Claims 69-71 were canceled with the Preliminary Amendment of January 14, 2005.

Claim 9

Applicants note that claim 9 is not listed in any rejection discussed in the Office Action. Therefore, Applicants respectfully note that if the Examiner intends to reject claim 9, he must do so in a new, non-final Office Action.

Rejections

Claims 1, 2, 4-8, 10-24, 31, and 34-37[1] are rejected under 35 U.S.C. § 102(e) as allegedly anticipated by Paton (U.S. Patent 6,703,277). Claims 25-29, 32, and 33 are rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Paton in view of Jeon (U.S. Patent 6,586,349). Claim 30 is rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Paton in view of Jeon and Green (U.S. Publication 2003/0219972).

Claim 1. Claim 1 requires, *inter* alia, an insulating film structure comprising: (a) "at least one silicon oxide region composed of a silicon oxide not containing said at least one metal

[1] At page 2 of the Office Action, the Examiner lists claims 1, 2, 10-26, and 31-37 in this rejection. However, in the rejection itself, claims 1, 2, 4-8, 10-24, 31, and 34-37 are discussed.

element"; (b) "at least one metal rich region having high concentration of said at least one metal element"; and (c) "at least one silicate region which is located between said silicon oxide region and said metal rich region and has a lower concentration of said at least one metal element that that of said metal rich region".

The Examiner asserts that layers 116, 120, and 108 of Paton anticipate these features of claim 1.

Paton is generally directed to a semiconductor device. Figures 2-5B illustrate the fabrication of a MOS structure. Figures 2-4B illustrate the deposition of an high-K dielectric material 108 on a silicon substrate 102, forming a interfacial silicon dioxide layer 118 therebetween. A metal layer 120 is deposited on the dielectric layer 108, and the gate layer 110 is deposited on the metal layer 120. The layers may then be etched to form the gate stack and sidewall spacers 114 as shown in Figure 4B. (col. 9, line 17 to col. 11, line 54) The resultant MOS structure of Figure 4B includes a metal layer 120, a high-K dielectric layer 108, and a interfacial silicon dioxide layer 118 between the gate electrode 110 and the silicon substrate 102. There is no disclosure that this structure includes a silicate region, between a metal layer and a silicon oxide region, having a lower concentration of a metal element than the metal layer. Rather, in the embodiment of Figure 4B, a dielectric layer is disposed between the metal layer 120 and the interfacial silicon dioxide layer 118.

Paton also describes that before or after etching the MOS structure of Figure 4A, the structure may be submitted to thermal processing, resulting in the structure of Figure 5B. Due to the thermal processing, the metal layer 120 diffuses through the dielectric layer 108 to reach the interfacial silicon dioxide layer 118. Thus, the unwanted silicon dioxide layer 118 is converted into a metal oxide layer 116. (col. 11, line 51 to col. 12, line 61) The resultant MOS structure of Figure 5B includes the high-K dielectric layer 108 and the metal oxide layer 116 between the gate electrode 110 and the silicon substrate. There is no disclosure that this structure includes a metal rich region or a silicon oxide not containing metal, as recited in claim 1.

Thus, neither the Paton device of Figure 4B, nor the Paton device of Figure 5B anticipates the limitations of claim 1. In his rejection, the Examiner appears to combine the metal layer 120 of the Figure 4B device with the metal oxide layer 116 of the Figure 5B device.

First, there is no disclosure or suggestion in Paton that this can be done. In order to form the structure of Figure 5B, the structure of Figure 4A or 4B is subjected to thermal processing which causes the metal layer to diffuse through the dielectric layer 108 and convert the unwanted silicon dioxide layer 118 into the metal oxide layer 116. There is no disclosure or suggestion of any structure including *both* the metal layer 120 *and* the metal oxide layer 116.

Additionally, even if the layers 120 and 116 were combined, they could only be comparable to the claimed metal layer and the claimed silicate region having less metal than the metal region. The metal oxide layer 116 is clearly described as including metal, and therefore

could not anticipate the claimed silicon oxide not containing metal, as alleged by the Examiner. Therefore, even if the layers 120 and 116 were combined (for which there is no disclosure or suggestion in Patton), there would still be no disclosure of a silicon oxide not containing metal, in conjunction with these layers.

Therefore, Applicants submit that Paton fails to anticipate claim 1.

Claims 2, 4-8, 10-24, 31, and 34-37. Applicants submit that these claims are patentable at least by virtue of their dependencies.

Claims 25-29, 32, and 33. Applicants submit that, as discussed in the Remarks section of the August 1, 2008 Amendment, neither Jeon nor Green makes up for the above-discussed deficiencies of Paton. Therefore, claims 25-29, 32, and 33 are also patentable at least by virtue of their dependencies.

In view of the above, Applicants respectfully request that the prior art rejections be reconsidered and withdrawn.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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